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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,190	01/20/2006	Masahiro Nomura	Q92733	9238

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
02/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/565,190	NOMURA, MASAHIRO	
	Examiner	Art Unit	
	HIEP NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-3,6,7,10,11,14, 18-26 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,10,11,14 and 18-26* is/are rejected.

7)☒ Claim(s) *29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 10-23-09 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3, 6, 8, 10, 11, 14 and 20-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "at least one first block receiving a variable supply voltage, said at least one first block receiving a clock signal; at least one second block receiving the variable supply voltage; and at least one variable delay circuit which provides a delay in the clock signal received by the at least one first block, said delay changing in accordance with a change in the supply voltage provided to the at least one first block; wherein the clock signal received by the at least one first block is different from a clock is different from a clock signal received by the at least one second block" is confusing because it is not clear whether the "at least one first block" or the "least one second block" receives the delayed clock signal. Assume that the "least one second block" receives the delayed clock signal for the art rejection. The recitation "the supply voltage" is confusing because it is not clear whether this "the supply voltage" is the same or different than the "variable power supply". This recitation lacks antecedent basis. The same rationale is applied to the recitation "the supply voltage" in claims 2, 3, 6, 7, 11, 22, 23, 25,

Regarding claim 3, the recitation "wherein the clock signal received by the at least on first block is different from the clock signal received by the at least one second block" is not clear what kind of clock signal the "at least on of the second block" receives.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Seno et al. (US. 6,924,679).

Regarding claim 1, figure 7 of Seno shows a multiple-supply-voltage semiconductor device comprising:

at least one first block (two first buffers of circuit 23) receiving a variable supply voltage (Vdd), said at least one first block receiving a clock signal (Sa);

at least one second block (24) receiving the variable supply voltage; and at least one variable delay circuit (two last buffer of circuit 23) which provides a delay in the clock signal received by the at least one second block, said delay changing in accordance with a change in the supply voltage provided to the at least one first block;

wherein the clock signal received by the at least one first block is different from a clock signal received by the at least one second block. Note that the variable power supply (26, 27) provides variable supply voltage to the circuit.

Regarding claim 2, it is inherent that when the power supply voltage decreases, the circuit perform slower thus, the delay increases.

Regarding claim 3, figure 7 of Seno shows a multi-supply-voltage semiconductor device comprising:

at least one first block (two first buffers of circuit 23) receiving a variable supply voltage, said at least one first block receiving a clock signal;

at least one second block (24) receiving the variable supply voltage;

a voltage level detector circuit (211) which detects a voltage level of "the supply voltage"; and at least one variable delay circuit (two last buffer of circuit 23) which provides a delay in the clock signal received by the at least one first block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein the clock signal received by the at least one first block is different from a clock signal received by the "at least one second block". Assume that the "at least one second block" receives the delayed variable clock.

Regarding claim 25, figure 7 of Seno shows a multi-supply-voltage semiconductor device comprising:

at least one block (two first buffers of circuit 23) receiving a variable supply voltage, said at least one block receiving a clock signal (Sa);

a voltage level detector circuit (221) which detects a voltage level of "the supply voltage"; and

at least one variable delay circuit (two last buffer of circuit 23) which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit; wherein said at least one variable delay circuit comprises a selector and a plurality of delay gates, wherein each one of said plurality of delay gates provides a different delay to the clock signal and the selector outputs to the at least one block either the clock signal or one of the delayed clock signals generated by the delay gate. Note that the variable power supply applied to circuit (221) varies the signal (Sa) that is in turn applied to the variable delay circuit thus; the delay changes in accordance with a change in the voltage level detected by the voltage level detector circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seno et al. (US. 6,924,679) in view of Masleid (2008/0303600).

Regarding claim 18, figure 7 of Seno includes all the limitations of these claims except for the limitation "multiple inverters connected in series" and "stacked inverter stage". However it is obvious that two non inverting buffer in series of Seno is equivalent to two inverters connected in series. Masleid, in paragraph [0049], discloses that the stacked inverter provides more input capacitance thus; it would have been obvious to one of ordinary skill in the art to replace the delay circuit with stacked inverter stages taught by Masleid for increasing the delay.

Allowable Subject Matter

Claims 10, 20, 21, 14, 24, 26 ,22,11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed on 11-06-09 have been fully considered but they are not persuasive. The newly added limitation "at least one second block" into claims 1 and 3 are not from claims 27 and 28.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIEP NGUYEN whose telephone number is (571)272-1752. The examiner can normally be reached on 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan Lam/
Primary Examiner, Art Unit 2816
/HIEP NGUYEN/
Examiner, Art Unit 2816
01-28-09